REMARKS/ARGUMENTS

Claim Rejections – 35 U.S.C. 102

Claims 13-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (Kim) US Patent No. 6,781,898 or rejected under 35 U.S.C. 102(a) as being anticipated by Chin US Patent Pub No. 2003/0145250.

Response:

Claim 13

In the Official action dated 12/19/2006, the Examiner rejected the currently pending claims 13-26 based on two cited references US 6,781,898, (Kim), and US 2003/0145250 (Chin), both of which were previously used for rejecting for substantially the same reason.

Particularly in finding the applicant's arguments unpersuasive, the Examiner states that "Kim discloses updating the linked list to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory (Fig. 3 and col. 6 lines 36-44) before the memory is completely examined by the BIST (Fig. 1b col. 5 lines 24-38 In other words, the linked listed[sic] is updated as each defective memory location is identified)." (Page 8 of the Office action dated 12/19/2006) The Examiner further states that "Chin discloses updating the linked list (block 12-15 and Fig. 4) to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory before the memory is completely examined by the BIST (Fig. 5[sic] loop between Refs. 21 and 24, and Fig. 5 loop between Refs. 32 and 34)." (Page 9 of the Office action dated 12/19/2006) The applicant respectfully disagrees.

The applicant once again would like to point out that the Examiner seems to have misinterpreted the disclosures of both the Kim reference and the Chin reference. The applicant will explain in more detail as follows. The applicant's invention discloses two

embodiments of a method for employing memory with defective sections in an electronic device, exemplarily in a network switch or router. For the purpose of explaining the two embodiments of the present invention, an exemplary device is shown in Fig. 2, wherein it includes a processor 50, a header table 20 for storing a linked list, a packet buffer 30 which contains pages of storage spaces corresponding to entries in the linked list, and an optional test result memory 40 for recording results of a BIST (paragraph [0017] of the originally filed specification).

While in the second embodiment as shown in Fig. 6 of applicant's invention, all the results of the BISTs are first stored into the test result memory 40 and then the linked list is formed in the header table 20 according to the stored BIST results in the test result memory 40; however, in the first embodiment as shown in Fig. 3 of applicant invention, an initially formed linked list is "dynamically" updated each time a defective section, either in the header table 20 or in the packet buffer 30, is found during the BISTs. When each update is processed, the BIST is paused, and the linked list is updated to remove the defective section. When the update is completed, the BIST is resumed. Due to the dynamic update nature of the first embodiment, the optional test result memory 40 is not even required. Please take note that because the applicant is aware of the similarity between the second embodiment of the present application and the cited references, i.e., Kim's and Chin's teachings, the claims of the present application have been amended to specifically cover only the first embodiment but not the second embodiment since the two cited references were first relied upon for rejection. In other words, the pending claims 13-26 are directed to the first embodiment only.

Regarding Kim's disclosure, Kim teaches a pointer memory 170 (or 102 shown in Fig. 1a and Fig. 1b), a data memory 190 (or 103 shown in Fig. 1a and Fig. 1b), and a defect marking memory implemented by the packet boundary memory 150. The applicant contends that, according to teachings of Kim, the functions of the pointer memory 170, the data memory 190, and the Defect Marking Memory 150 actually respectively resemble those of the header table 20, packet buffer 30, and test result memory 40 of the

present application. The operations taught by Kim are best illustrated in the flowchart of Kim Fig. 3, where the flow is divided into three phases: Defect-Marking-Memory Test process 201, Defect Row Marking process 202, and Defect Row Skipping process 203. The applicant further contends that the Defect Row Marking process 202 resembles the BIST labeled as 200 and/or 220 in Fig. 6 of the second embodiment of the present application, and the Defect Row Skipping process 203 resembles the linked list formation labeled as 240 in Fig. 6. As one can see, the Defect Row Skipping process 203 is started only after the condition of step 234 is met. In other words, the Defect Row Skipping process 203 is not actuated until all addresses of other memories, including the pointer memory 170 and the packet data memory 190, are tested. This is also described in col. 6 lines 32-33, "Once all addresses are tested, 234, the process shifts to a Defect Row Skipping process," which is basically what has been taught in the second embodiment of the present application, but not in the first embodiment to which claim 13 is directed. Even the paragraphs where the Examiner relied upon in asserting rejection concurs the applicant's position. In col. 6 lines 36-44 of Kim, it is stated that "the Defect Row Skipping process informs the Linked List Initializer 166 in FIG. 2 of **all the defective addresses**" (emphasis added), and it becomes clear that all the defective addresses are made available before the linked list is initialized, rather than that a linked list is first formed and then updated dynamically. Therefore, the applicant asserts the claimed feature "**updating the linked list** to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory **before the memory is completely examined by the BIST**" (emphasis added) is neither taught nor suggested by Kim's teachings.

Regarding Chin's disclosure, Chin teaches in Fig. 3 a packet buffer 1 and a so-called free link table 2, which shows a one-to-one mapping relationship with the data rows of the packet buffer 1. Although the naming convention of the free link table 2 easily leads one to understand it as a linked list, and indeed the disclosure of Chin is ambiguous and confusing in this respect, the applicant nevertheless contends that the function of the free

link table 2 in Chin actually resembles that of the test result memory 40 of the present application for storing defective sections, but not that of the header table 20 of the present application for forming the linked list. Referring to Chin Fig. 4, in this embodiment Chin first performs a BIST to see whether data rows in the packet buffer 1 are defective, and when a defective row is found, the block in the free link table 2 corresponding to said data row will be recorded as fail, otherwise recorded as good. After all blocks in the free link table 2 are marked, all records of the free link table 2 will then be read out and only those blocks recorded as good will be initialized. While in the embodiment shown in Chin Fig. 5, it is different only in that the blocks in the free link table 2 are initially preset as good, and only those mapping to defective data rows are changed to fail. The choice of language such as "record", "marked", "read" used together with the free link table 2 obviously indicates that the free link list 2 is used for the purpose of defect marking or defect recording, and will be later read when all of the defects are detected and recorded (that is, upon completion of BIST), as a reference for forming, or initializing, a linked list. Therefore, it is immaterial to the patentability of claim 13 that in Fig. 5 Chin teaches default-recording all blocks in the free link table as good and then changing to fail upon locating a defective data row, because in the end Chin still only discloses performing BIST and recording the results of BIST, but not dynamically updating an already formed linked list. Therefore, the applicant asserts the claimed feature "**updating the linked list** to remove from the linked list the entry of the linked list corresponding to the identified first defective portion of the memory **before the memory is completely examined by the BIST** (emphasis added)" is neither taught nor suggested by Chin's teachings.

In light of above arguments, the applicant believes that claim 13 has overcome the rejections and placed in condition for allowance.

Claims 14-18

In the listing of claims presented in the previous response, filed on 11/17/2006 and requesting continued examination, claim 16 has been cancelled by the applicant.

Updating of the claims presented for examination is respectfully requested.

Claims 14-15 and 17-18 are dependent upon claim 13, and should be allowed if claim 13 is found allowable.

Claim 19

In light of above arguments under Claim 13, the applicant asserts that the claimed feature "the step of updating the linked list is performed before the memory is completely examined by the BIST" is neither taught nor suggested by Kim's and Chin's teachings. Reconsideration of claim 19 is respectfully requested.

Claims 20 and 21

Claims 20 and 21 are dependent upon claim 19, and should be allowed if claim 19 is found allowable.

Claim 22

Claim 22 recites that "(d) after step (c) is completed, continuing the BIST to identify a second defective portion of the memory." Please note that, "continuing the BIST" means that the BIST is **NOT** completely finished. In light of above arguments under Claim 13, the applicant therefore asserts that claim 22 has overcome the rejections.

Claims 23 and 24

Claims 23 and 24 are dependent upon claim 22, and should be allowed if claim 22 is found allowable.

Claim 25

Claim 25 recites that "each time a defective portion is found in the memory by the BIST, **pausing** the BIST, **updating the linked list** to remove an entry corresponding to the defective portion of the memory from the linked list, **and then continuing the BIST**

on remaining portions of the memory (emphasis added)." As explained previously, it can be readily derived from the limitations specified in claim 25 that the operation of updating the linked list begins **BEFORE** the time at which the BIST is completely finished. In light of above arguments under Claim 13, the applicant therefore asserts that claim 25 has overcome the rejections.

Claim 26

Claim 26 is dependent upon claim 25, and should be allowed if claim 25 is found allowable.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 03/19/2007

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

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